Applicant: Kassem M. Abdallah, *et al.*
U.S.S.N.: 10/737,305
Filing Date: December 16, 2003
EMC Docket No.: EMC-03-104

REMARKS

In response to the Final Office Action mailed May 31, 2006, the applicants respectfully request reconsideration. In the Office Action, Claims 5-12, 18-24, 26, and 27 were objected to and Claims 1-4, 13-17, 25, and 28-31 were rejected. By this amendment Claim 1 has been amended to include all of the limitations of Claim 5 and Claim 5 has been canceled. Claim 6 has been amended to depend from Claim 1.

Claims 1-4 and 6-31 are pending in the application.

Claim Rejections – 35 U.S.C. § 102

Claims 1-4, 13-17, 25, and 28-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,872,980 ("Derrick").

With respect to Claims 1-4, Claim 1 has been amended to include all of the limitations of Claim 5, which examiner indicated would be allowable if rewritten in independent form including all of the limitations of the base claim. Claims 2-4 and 6-12 now depend from amended Claim 1 and the applicants respectfully assert that all of these claims are in condition for allowance.

The rejection of Claims 13-17, 25, and 28-31, including independent Claims 13 and 28 is respectfully traversed, as Derrick does not teach every element of the claims, as is required for a proper rejection under § 102.

Independent Claim 13 recites:

> A controller for arbitrating access to at least one shared resource by a plurality of processors, the controller comprising:
>
> a first register portion including a plurality of layers, each of the plurality of layers being associated with a different one of the plurality of processors, each of the plurality of layers including an access indication portion associated with each of the at least one shared resource, the access indication portion holding an indicator of whether a processor associated with a particular layer has obtained

> access to communicate with the shared resource associated with the access indication portion of the particular layer; and
>
> an access arbitration device associated with all of the access indication portions of each of the at least one shared resources for controlling access to the associated shared resource by the plurality of processors, the access arbitration device including an input for receiving access indication signals from the plurality of processors, the access arbitration device:
>
> (A) determining whether the at least one shared resource is being accessed by any of the plurality of processors; and
>
> (B) arbitrating access to the shared resource based on the determination made in Step (A).

The applicants respectfully assert that Derrick does not teach or suggest a first register portion including a plurality of layers, each of the plurality of layers being associated with a different one of the plurality of processors. The examiner asserts that the plurality of stacked registers in Derrick is the equivalent of the plurality of layers recited in Claim 13. However, the examiner also asserts that "it is clear that each ID field in the memory location (register) is associated with each of the plurality of processors, and the lock bit(s) indicates whether any of the processors has obtained access to the shared resource.

The registers in the spin buffer described in Derrick are not the equivalent of the layers recited in Claim 13. As described in the Specification at page 9, line 22 to page 10, line 23, and shown in Figure 1, the blocks (each of which represents a bit) with the numbers 0-15 in them are all part of layer 23a, which is associated with processor P0. Additional layers 23b, 23c, and 23d are each associated with another one of the processors (P1, P2, and P(m-1), respectively), and each layer also includes its own bits 0-15. Each of the bits in the layers corresponds to one of the shared resources. However, as indicated by the Examiner in the Office Action, only individual bits in the registers disclosed by Derrick are associated with the processors (Derrick Column 5, lines 9-33). Thus, the registers in Derrick are setup differently than the layers in the present invention. Instead of a plurality of layers (registers) that are associated with the processors, each

layer including a bit associated with each of the shared resources, Derrick describes a plurality of registers that are associated with the shared resources, each register possibly including a bit associated with each of the processors.

Furthermore, the applicants respectfully assert that Derrick does not teach or suggest a controller comprising, in part, "an access arbitration device . . . for controlling access to the associated shared resource by the plurality of processors" that functions as claimed. The controller claimed here includes one access arbitration device per shared resource ("an access arbitration device associated with all of the access indication portions of each of the at least one shared resource"). For a better understanding of this access arbitration device, the examiner is invited to look at Figure 1. Devices 24a, 24b, 24c, 24d, and 24m are each access arbitration devices, the details of which are shown in Figure 2 (Specification page 11, lines 12-13). Each arbiter deals with requests for only one of the shared resources (Specification page 11, lines 13-16). This is different than the arbiter, 506, shown in Derrick, whose function is not described. Derrick only shows one arbiter that is not associated with any of the shared resources, contrary to the arbitration device recited in Claim 13.

Also, the controller in Derrick does not receive access indication signals from the processors. These signals (lock bits) may either be a 1 to indicate that the processor is requesting access to the shared resource (see Specification page 12, lines 8-13) or a 0 to indicate that the processor is not requesting access to the shared resource (see Specification page 12, lines 15-17) or that the processor is relinquishing access to the shared device (see Specification page 13, lines 22-24). There is no teaching or suggestion in Derrick of such a signal. The controller described in Derrick instead works by detecting a read for ownership of the shared resource (Derrick Column 5, lines 34-39). This same "read for ownership" is not the same signal that is used by the

applicants' processors to relinquish control over a shared device as recited in Claim 13. Instead, the processors in Derrick must "clear[] the lock bit (step 310), which relinquishes ownership of the shared resource (step 312)" (Derrick Column 4, lines 22-23). Therefore, there is no access indication signal taught or suggested in Derrick.

Therefore, Derrick does not teach or suggest all of the elements of Claim 13. Derrick does not teach or suggest a register including a plurality of layers associated with each of the processors, each of the layers including an access indication portion associated with each of the shared resources. Derrick also does not teach or suggest an access arbitration device associated with each of the shared resources, nor does Derrick teach or suggest an access indication signal that is used by such a device. The applicants therefore respectfully assert that Claim 13 is allowable over Derrick, and that the rejection of Claim 13 under 35 U.S.C. § 102 should be withdrawn.

Claims 14-17 depend from independent Claim 13 and are allowable for at least the same reasons as Claim 13, as argued above.

Independent Claim 28 recites:

> A method of arbitrating access to a shared resource by a plurality of processors, the method comprising:
> A) processing access indication signals received from each of the plurality of processors;
> B) storing the processed access indication signals;
> C) performing a logic operation on the processed access indication signals to generate an access arbitration signal;
> D) receiving a further access indication signal from a particular one of the plurality of processors; and
> E) arbitrating access to the shared resource by the particular processor based on the state of the access arbitration signals.

The applicants respectfully assert, as set forth above, that Derrick does not teach or suggest access indication signals received from each of the processors.

Furthermore, even if Derrick did teach or suggest access indication signals received from each of the processors, he does not teach or suggest processing and storing those signals and then performing a logic operation on those signals to generate an access arbitration signal, as recited in Steps A, B, and C, respectively. For a better understanding of this method of arbitration, the examiner is invited to look at Figure 2 and the description thereof.

The only information that Derrick describes as being stored is the ID and lock information in the spin buffer. The ID information is an identification of the bus master that currently owns the resource (Derrick Column 5, lines 7-8). The lock information is an indication of whether the shared resource is owned by a bus master (Derrick Column 5, lines 4-7). Neither of these pieces of information are processed access indication signals. Rather, they are the final result of the arbitration performed by the mechanism described in Derrick. They are only written once a determination is made as to whether the shared resource is already owned or not (Derrick Column 5, lines 41-51).

This is contrary to the method described in the current application and recited in Claim 28. Here the arbiter receives a signal, processes it at AND gate 26 by combining it with the output of inverter 39, which is the inversion of the output of OR gate 37, the access arbitration signal, and stores it using demultiplexer 28 into one of the bits 33a-33d. Only then is an access arbitration signal generated by ORing the bits 33a-d. Using this method, anytime an access arbitration signal is received it is processed and the result is stored in the appropriate bit 33a-33d. Using the method of Derrick, the only time information is stored is when a device is assigned to own a shared resource. Therefore Derrick cannot and does not disclose Steps A-C of Claim 28. Accordingly, since Derrick does not teach or suggest all of the elements of the Claim 28, the

applicants respectfully assert that Claim 28 is allowable over Derrick and that the rejection of Claim 28 under 35 U.S.C. § 102 should be withdrawn.

Claims 29-31 depend from independent Claim 28 and are allowable for at least the same reasons as Claim 28, as argued above.

Claim Objections

Claims 5-12, 18-24, 26, and 27 were objected to as being dependent upon a rejected base claim. Claim 5 has been canceled and its features have been incorporated into amended Claim 1. Claim 6 has been amended to depend from Claim 1 instead of canceled Claim 5. The applicants therefore respectfully assert that Claims 1-4 and 6-12 are in condition for allowance and request that the objection be withdrawn.

With respect to Claims 18-24, 26, and 27, the applicants respectfully assert that Claim 13, from which these claims depend, is allowable in view of the arguments above and that there is no need to rewrite the claims objected to in independent form. The applicants therefore respectfully request that the objection be withdrawn.

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Conclusion

In view of the foregoing, the applicants assert that Claims 1-4 and 6-31 are in condition for allowance and respectfully request favorable reconsideration.

In the event the examiner deems personal contact desirable in the disposition of this case, the examiner is invited to call the undersigned attorney at (508) 293-7835.

Please charge all fees occasioned by this submission to Deposit Account No. 05-0889.

Respectfully submitted,

7/31/06
Date

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